

Techniques of Improving Electric Characteristics of Si Strip Sensors Equipped using Various Isolation Methods

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ABSTRACT

Si sensors in future generations of accelerators will face a harsh radiation environment. Additionally, the double-sided silicon sensors are having an electron accumulation layer between the n+ strips in the p+-n--n+ configuration. Various techniques, like p-spray and p-stop, which provide interstrip isolation, have an additional impact on other properties of sensors including capacitance and breakdown voltage. The p-spray has good interstrip trends, but isolation ensuring p-spray dose leads to very poor VBD. P-stop doping (\sim 1018 cm-3) ensures strip isolation but leads to high inter-strip capacitance and low VBD, particularly for high surface damage. Thus, to find out the optimized electric characteristics of the p+-n--n+ sensors, a simulation-based comprehensive analysis is performed for a combination of these two techniques.

Keywords: Si Sensors, Strip Isolation, Simulation, P-stop, P-spray

INTRODUCTION

i strip sensors are widely used in present-day nuclear and particle physics experiments [1]. Double-sided Si Strip Detectors (DSSDs) can be useful for particle tracking purposes due to their durability and low mass tracker design required. However, a positive oxide charge density $Q_{\scriptscriptstyle E}$ (~ 10^{11} cm⁻²) is produced around the Si-SiO₂ interface of the sensor. Further, during the detector operation, high energy radiation introduces bulk damage [2] in sensor volume and at the Si-SiO2 interface, causing surface damage [3], leading to an increase in Q_E up to a high value of around 3x10¹²cm⁻² shorting the adjacent n+-strips, leading to loss of position resolution. Surface damage can affect the operational characteristics of silicon sensors. The presence of Q_E near the Si-SiO₂ interface results in the formation of an electron accumulation layer just below the Si-SiO, interface. The increment in the value of Q_F after exposure to ionizing radiation results in a denser electron accumulation layer. The dense electron accumulation layer results in various degrading effects for silicon sensors. For p-on-n sensors (with p+ pixel or strip implants), a dense electron accumulation layer creates high electric eld regions near p+ doping. These high electric field regions may decrease the breakdown voltage for the irradiated p-on-n strip/pixel sensors.

Further, the presence of a dense accumulation layer creates non-depleted regions between the strips/pixels, which may result in a reduction of signal for particles hitting between the strips/pixels. Further, surface damage results in an increase in interstrip capacitance (C_{int}) , and affects the breakdown voltage (V_{BD}) of Si sensors.

For the n+ side of double-sided strip sensors, the strip isolation problem can be resolved by introducing p-stop [4] and p-spray [5] under SiO₂. However, using these strategies adversely affects the V_{BD} and C_{int} of the sensors. It has been shown that [6] individual p-stop or p-spray techniques do not provide an adequate solution. In this work, a comprehensive simulation study of the combination of these two isolation techniques, along with various numbers of p-stops and p-stops with metal overhang for the ohmic side of p+-n--n+ sensors, is carried out for different designs. For this work, we have used Q_E values from 1x10¹¹ cm⁻² (non-irradiated sensor) to 3x10¹² cm⁻² (highly irradiated sensor). Present work may be useful for surface damage; however, bulk damage effects should also be considered for the proper simulation of sensors. The proposed design guideline is a tradeoff between interstrip conductance G_{int}, C_{int} and $V_{\rm BD}$.

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The silicon sensor device simulations using the TCAD (Technology Computer Aided Design) software have become an indispensable tool in the development of radiation-hard silicon sensor designs. The Silvaco and Synopsys TCAD tools [7, 8] are the common software used by the silicon sensor community. These TCAD software are widely used in the semiconductor industry, and their simulation capabilities have been well tested for different silicon device designs over many years. These TCAD tools have a significantly large user base and can be used with ease. The proliferation of TCAD tools in silicon sensor development is due to some of the reasons outlined below:

- (a) The TCAD simulations help in predicting the various properties of silicon sensors under operating conditions without actual device fabrication. Using these simulations, it is possible to visualize the effect of variation of particular sensor parameters (say bulk doping) on different sensor properties (electrical, thermal and optical properties). So, these simulations allow the optimization of sensor fabrication process and geometrical design parameters, which would be a very difficult task using experimental investigation only.
- (b) These TCAD tools can be used to simulate the radiation damage using the appropriate bulk and surface damage models. Using these TCAD software, it 40 is possible to mimic the bulk damage by implementing the different trap levels inside the band gap of silicon. Moreover, surface damage can be implemented using the appropriate oxide charge density and interface traps along the SiSiO₂ interface. The TCAD simulations can be used to understand the radiation dam age mechanism on silicon sensors by comparing various macroscopic quantities like electric elds, electron/hole currents, space charge density etc. inside the sensor volume under different operating conditions and irradiation fluence.

Present simulations are performed with the help of a semiconductor device simulator, ATLAS [7].

DESIGN STRUCTURE AND SIMULATION TECHNIQUE

Simulations are performed on a n-type substrate having bulk doping of 7×10^{11} cm⁻³, thickness of $300\mu m$ with n^+ strips of $18\mu m$ and strip pitch of $80\mu m$. The n^+ and

 p^+ depths are kept at $1 \mu m$ (where concentration is equal to bulk n^-) with the Gaussian profile.

The schematic of the structures simulated in this work is shown in Figure 1. Set A defines the basic reference structures with p-stop and p-spray isolation techniques. A1 defines a p-spray structure with a peak doping concentration of 2.8×10^{17} cm⁻³ and a doping depth of $0.5\mu m$. In contrast, A2 defines a structure with a 40m wide single p-stop with a doping concentration of 1×10^{18} cm⁻³ and a p-stop doping depth of $1\mu m$. Set B contains symmetrically placed double p-stop structures (B1) separated by $d_1 = 12\mu m$ along with triple p-stop structures (B2) separated by $d_2 = 11\mu m$. As distances between the outer edges of outer p-stops are always equal to $40\mu m$, all the configurations can be considered equivalent to $40\mu m$ single p-stop and hence are compared in this work.

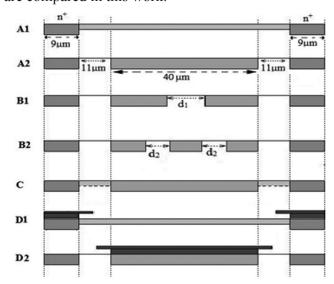


Fig. 1. Schematics of the simulated strip sensors with different isolation structures

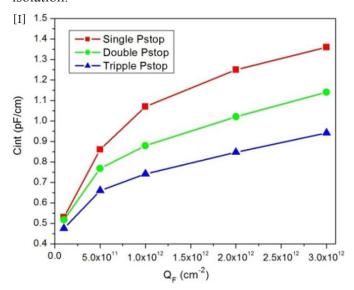
Set C defines p-stop – p-spray combined isolation in which a $40\mu m$ wide p-stop with a doping depth of 1m on a p-spray layer of doping depth of 0.5 μm is considered. The effect of metal overhang over p-spray and p-stop is quantified using structures D1 and D2, respectively. All these structures have good strip isolation properties, so only C_{int} and V_{BD} comparisons are shown in the results section.

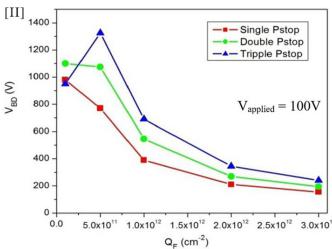
SIMULATION RESULTS

Multiple P-stop isolation

 C_{int} vs. Q_F plot for multiple P-stops is shown in figure 2(I). For all the configurations, an increase in Q_F

results in an increase in the electron accumulation concentration, which leads to a narrower depletion width between n-substrate and p-stop and hence causes a higher value of C_{int}. A structure having single p-stop (A2) has the highest Cint as compared to double (B1) and triple (B2) p-stops since, in latter cases, additional capacitors in series lead to lower Cint. It can be observed from figure 2(II) that a single p-stop set (A2) has the lowest VBD, followed by double and triple p-stops. Thus, triple p-stop provides better C_{int} and V_{BD} performance than single p-stop while ensuring isolation.



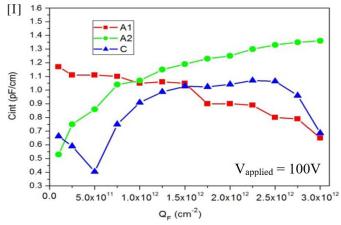


 $\textbf{Fig. 2.} \ (I) Plot \ of \ C_{_{int}} \ vs \ Q_{_{F}}, \ and \ (II) \ Plot \ of \ V_{_{BD}} \ vs. \ Q_{_{F}}, \ for$ the different multiplicity of p-stops

P-stop – P-spray Combined Isolation

Simulations have found that for $N_{pspray} = 4 \times 10^{16} \text{ cm}^{-3}$ and $N_{pstop} = 1 \times 10^{17} \text{ cm}^{-3}$, the most optimized results of C_{int} and V_{BD} are achieved which are shown as set C in

figure 3. For comparison, plots of A1 (p-spray) and A2 (p-stop) are also shown.



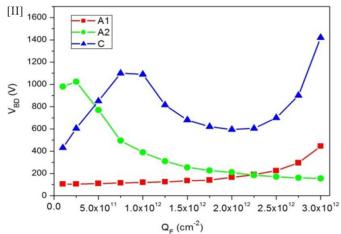


Fig. 3. (I) Plot of G_{int} vs. Q_F , and (II) Plot of V_{BD} vs Q_F , for p-stop – p-spray combinations

P-spray/P-stop with Metal Overhang (MO)

Since the metal overhang is directly coupled to the electron accumulation layer below it, forming a parallel

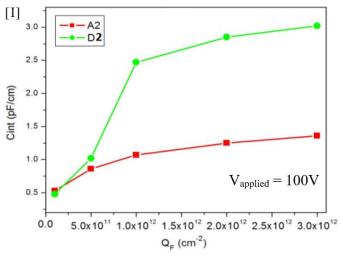


Fig. 4. (I) Plot of C_{int} vs. Q_F at $V_{applied} = 100 V$

capacitor, its introduction results in a significant increase in $C_{\rm int}$ (Figure 4(I)) both for D1 and D2 configurations. The metal overhang structure is useful in increasing the $V_{\rm BD}$ for D1 and D2 for intermediate values of $Q_{\rm F}$. As the metal overhang structure is tied with p-stop in D2, it has a negative potential compared to the electron accumulation layer. This results in the smoothening of potential contours, thus increasing the $V_{\rm BD}$ (Figure 4(II)).

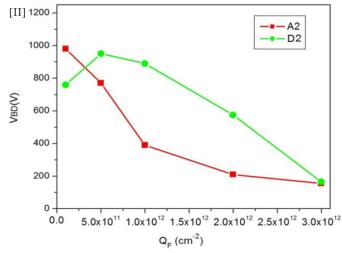


Fig. 4. (II) Plot of V_{BD} vs Q_{F} , for A2 and D2 structures

SUMMARY AND CONCLUSION

The P-stop and p-spray are commonly used techniques for strip isolation on the n⁺ side of the p⁺–n⁻–n⁺ Si strip sensors. Here, we have investigated the effect of other alternative designs, which include one or more p-stop, p-spray – p-stop combinations and metal overhangs. It

is found that using multiple p-stops improves the Cint and $V_{\rm BD}$ without degrading $G_{\rm int}$. Similarly, optimized p-spray – p-stop combined isolation has good $C_{\rm int}$ and $V_{\rm BD}$ without losing strip isolation. The use of metal overhang over p-stop to improve $V_{\rm BD}$ is not an attractive option as it results in significant deterioration of $C_{\rm int}$.

ACKNOWLEDGEMENTS

The author would like to thank Prof. Ashutosh and Kirti Ranjan from the CDRST lab at the University of Delhi for their insightful guidance in this work.

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